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SIMULATION AND PARAMETER EXTRACTION OF CMOS DEVICES

R. Wada[1], H. R. J. Grados[2], J. A. Diniz[2]

[1]Faculty of Electrical and Computer Engineering, State University of Campinas,
[2]Center for Semiconductor Components (CCS), State University of Campinas
wada@fee.unicamp.br

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ABSTRACT

The parameter extraction of CMOS devices finds a wide set of applications and interests in microelectronic industry. Essentially, this work presents methods used for simulation and parameter extraction of CMOS devices, such as mathematical analysis and computer simulation. The mathematical analysis is based on graphical studies of the current, voltage and capacitance curves of the measured components. Then, with the variables available several parameters are extracted through mathematical equations. The computer simulation is performed by the software *Advanced Design Systems* (ADS). Due to its wide capability to optimize parameters, the ADS allows the user to obtain these parameters through iterative simulations, until the desirable error is reached.

MATHEMATICAL ANALYSIS

The mathematical analysis were based on the results obtained from NMOS transistors with different length channels (L) fabricated in Center for Semiconductor Components (CCS). All of these components have the width channel (W) of 20µm. In Figure 1, it can be seen the main structure of a NMOS transistor, where V_G, V_D, V_S and V_B are respectively the gate, drain, source and bulk voltages. Figure 2 presents the transconductance (g_m) x V_{GS} curves obtained from the I_D x V_{GS} measurements, where I_D is the drain current. With the maximum g_{mMAX} values (extracted from curves of Figure 2), it can be seen in Figure 3 (W/g_{mMAX} x L curve) graphical method to determine the effective length channel (L_{eff}), following the expression: Leff = L – ΔL, where ΔL value is shown Figure 3. Figure 4 shows the capacitance curve of the gate terminal and finally Table 1 summarizes how these data can be combined together to find the electron mobility.

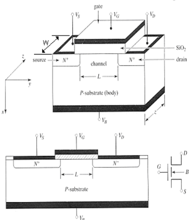
Figure 1

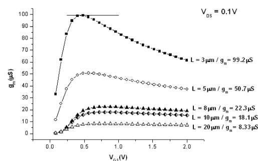
Figure 2

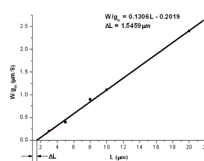
Figure 3

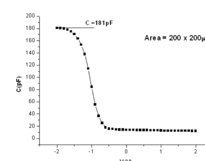
Figure 4

Electron mobility: $\mu_N = \dfrac{L_{eff}}{W.C_{OX}.V_{DS}} g_m$

Table 1

L (µm)	μ_N (cm²/Vs)
10	169
5	137
3	172

COMPUTER SIMULATION

Figures 5 and 6 show the necessary layouts to implement the computer simulation by ADS. In Figure 7 we can see the curves I_D x V_{DS} of a NMOS transistor with L = 5µm for different values of V_{GS}. As we can see, a good evaluation of parameters in simulation happens when the curves measured and simulated became coincident.

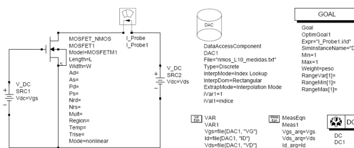
Figure 5

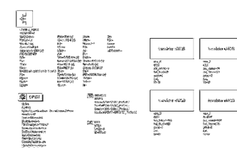
Figure 6

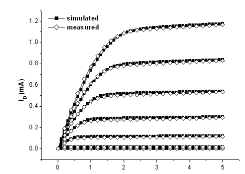
Figure 7

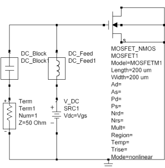
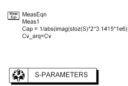
Figure 8

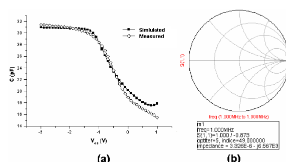
Figure 9

The simulation of the capacitor was done according to structure in Figure 8. In laboratory, the capacitance analyzer equipment was responsible to provide a constant frequency of 1MHz while the gate voltage (V_{GS}) was varied from –3 to 1V. For simulate these identical conditions, we used a frequency source that is represented by a resistance of 50Ω. In Figure 9, (a) shows the curves simulated in ADS and measured in laboratory and (b) presents its Smith Chart.

RESULTS

Several parameter extractions by mathematical and computer methods were proposed and evaluated in this study. There is a high potential of studies in this area, and their applications are very promising in electronic industry. The program ADS provided a powerful tool in simulation and optimization processes. Also we have observed that each model, such as SPICE and BSIM, was suitable according to its application. For the transistor optimization, the SPICE model was sufficient to provide us all the basic parameters and we had to use the BSIM model to capacitor simulation.

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